ADFP Cloud 3.0

Full-custom 設計使用者手冊

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目錄

1. ADFP Cloud 3.0 PDK 下載與安裝

1.1 拷貝製程資料夾

目標資料夾:

/RAID2/PROCESS/ADFP/Executable_Package/Collaterals/Tech/iPDK/N16ADFP_iPDK/

[~]$ cd ~

[~]$ mkdir ADFP

[~]$ cd ADFP

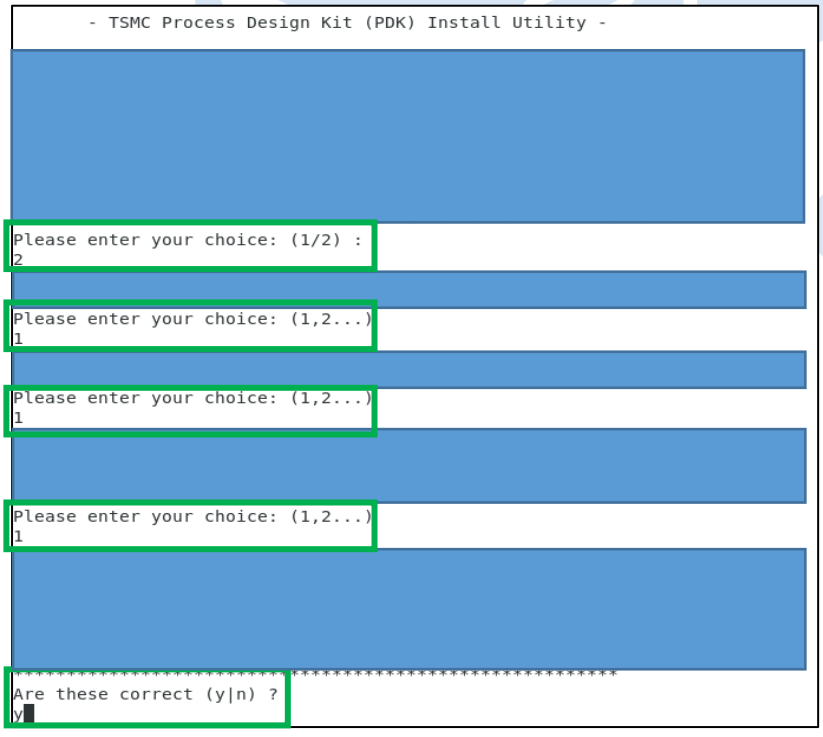
[~/ADFP]$ cp -r /RAID2/PROCESS/ADFP/Executable_Package/Collaterals/Tech/iPDK/N16ADFP_iPDK/ .

1.2 安裝 PDK (必要步驟)

於該資料夾中執行 ./pdkInstall.pl，並依序輸入 「2, 1, 1, 1, y」

[~/ADFP]$ cd N16ADFP_iPDK

[~/ADFP/N16ADFP_iPDK]$ ./pdkInstall.pl



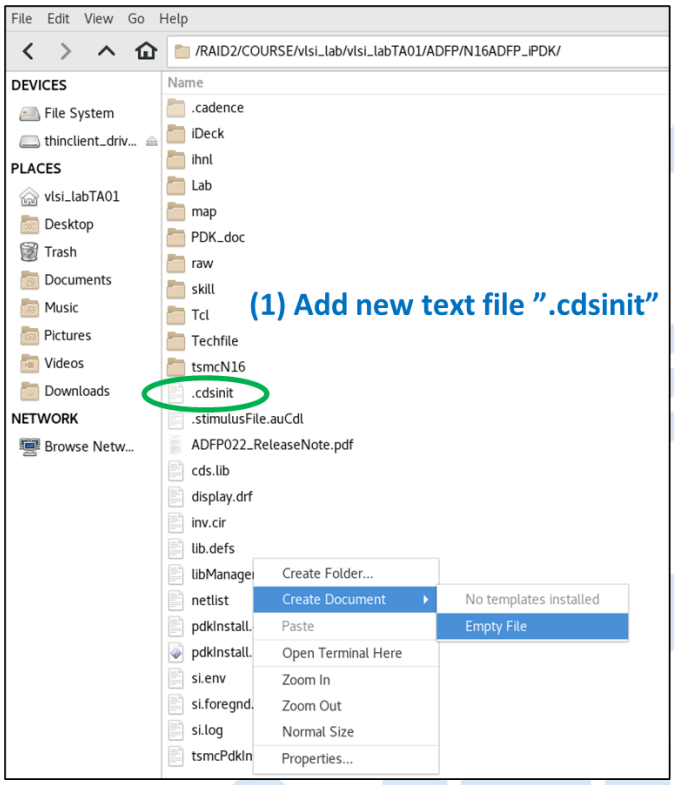
1.3 確認是否正確完成安裝

出現以下畫面代表成功安裝

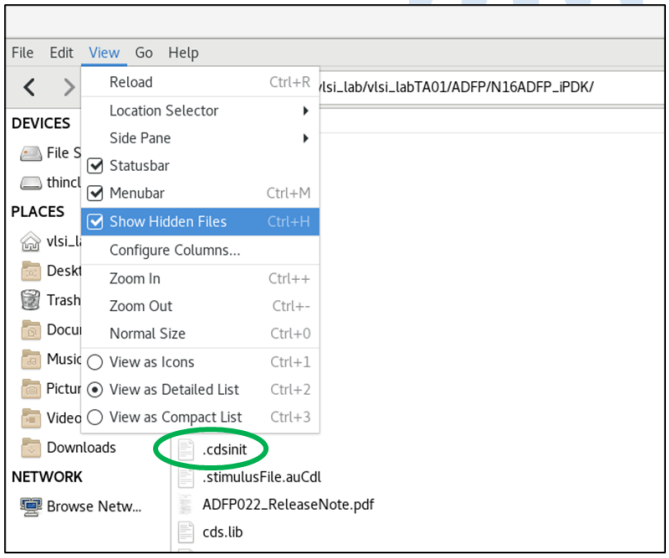
```
*Info: PDK installation completed.
15:13 vlsi_labTA01@cad11[~/ADFP/N16ADFP_iPDK]$
```

1.4 創建並修改.cdsinit 檔案

(1) 在 N16ADFP_iPDK 資料中，新增「.cdsinit」檔案



(2) 將隱藏的檔案顯示



(2) Show hidden file to find ".cdsinit"

(3) 打開檔案並加入以下文字，這會讓 Calibre 加入 Virtuoso 畫面中

;Set Calibre Path

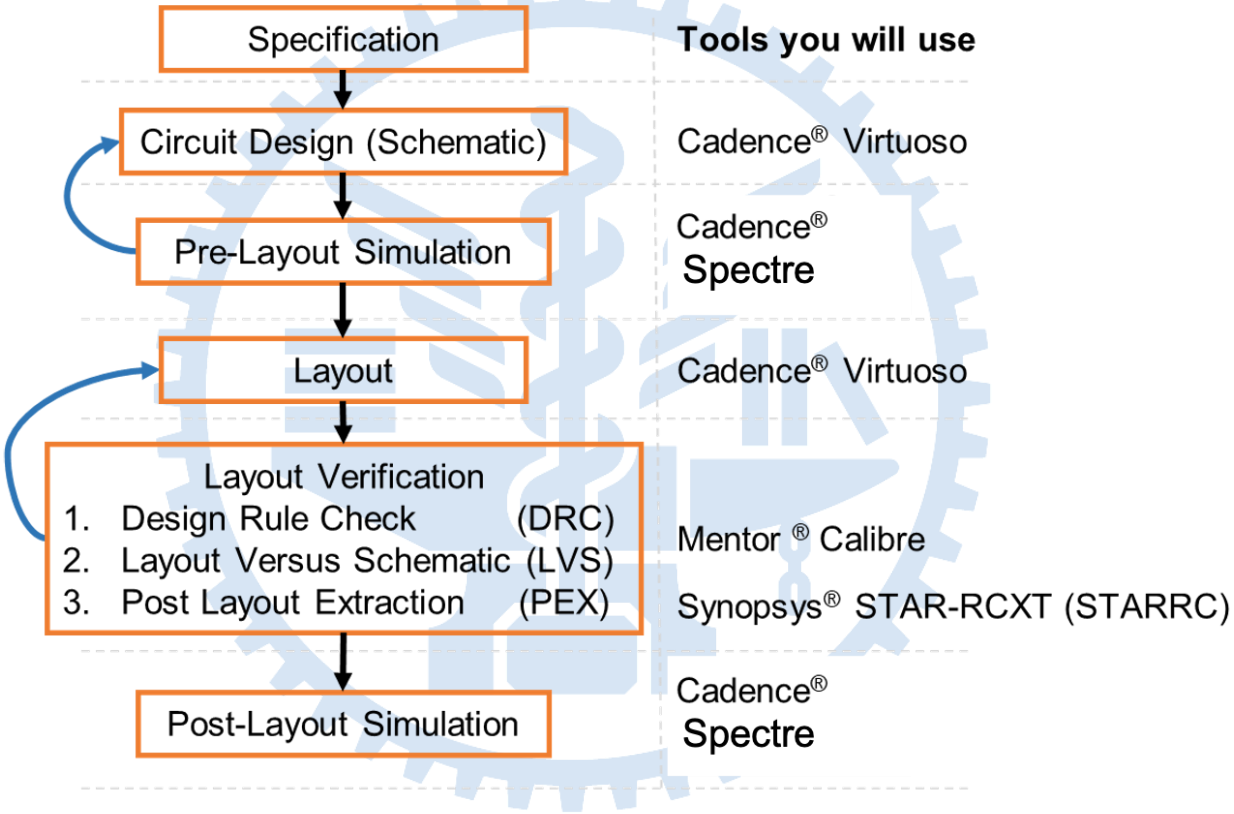
setSkillPath(“ /RAID2/cad/mentor/calibre/cur/shared/pkgs/icv/tools/queryskl”)

load(“calibre.skl”)

```
bash-4.4$ cat .cdsinit
setSkillPath(" /RAID2/cad/mentor/calibre/cur/shared/pkgs/icv/tools/queryskl")
load("calibre.skl")
```

1.5 安裝完成^w^

1.6 在這個範例教程，將會使用以下 EDA 工具作為教學



2. Circuit Design (Schematic)

2.1 裝載所需的 EDA Tool 環境

打開 Terminal 輸入以下指令查看工作站上的所有 EDA tool 環境

[~/ADFP/N16ADFP_iPDK]$ module avail

```
bash-4.4$ module avail

------------------------------------------------------ /RAID2/modulefiles/other ------------------------------------------------------
   calibre/2019.2_26.18    calibre/2025.3_28.17 (D)    matlab/R2021    vscode/default       vscode/2025.12.19 (D)
   calibre/2025.2_14.11    matlab/R2021a        (D)    uv/0.8.17       vscode/2025.09.16

----------------------------------------------------- /RAID2/modulefiles/synopsys -----------------------------------------------------
   customcompiler/2025.06-2        fc/2025.06          icc2/2025.06       primesim/2025.06-1          tmax/2025.06
   customexplorer/2025.06-2        finesim/2025.06-1   icc3d/2025.06      primetime/2025.06           vcs/2025.06
   customsim/2025.06-1             formality/2025.06   icv/2025.06-1      spyglass/2025.06            verdi/2019.06
   dc/2022.03                      hspice/2025.06-1    laker/2024.12-2    starrc/2019.12-sp5-3 (D)    verdi/2022.06
   dc/2025.06              (D)     icc/2025.06         lc/2025.06         starrc/2025.06              verdi/2025.06 (D)

----------------------------------------------------- /RAID2/modulefiles/cadence ------------------------------------------------------
   genus/21.18.000              jasper/2024.03p002    quantus/23.11.000    tempus/23.14.000               virtuoso/23.10.140
   innovus/DDI_23.34.000 (D)    liberate/23.16.074    spectre/23.10.802    verisium/24.09.002             vmanager/24.03.004
   innovus/21.19.000            pegasus/21.20.000     stratus/24.02.003    virtuoso/ICADVM_20.10.340 (D)  xrun/24.09.006

----------------------------------------------------- /RAID2/modulefiles/common -------------------------------------------------------
   base/all (D)    base/cb    base/fc_old    base/fc    license/all (D)    license/lshc    license/lstc    license/lstn    site/iclab

---------------------------------------------- /usr/share/lmod/lmod/modulefiles/Core ----------------------------------------------
   lmod    settarg

  Where:
   D:  Default Module

If the avail list is too long consider trying:

"module --default avail" or "ml -d av" to just list the default modules.
"module overview" or "ml ov" to display the number of modules for each name.

Use "module spider" to find all possible modules and extensions.
Use "module keyword key1 key2 ..." to search for all possible modules matching any of the "keys".
```

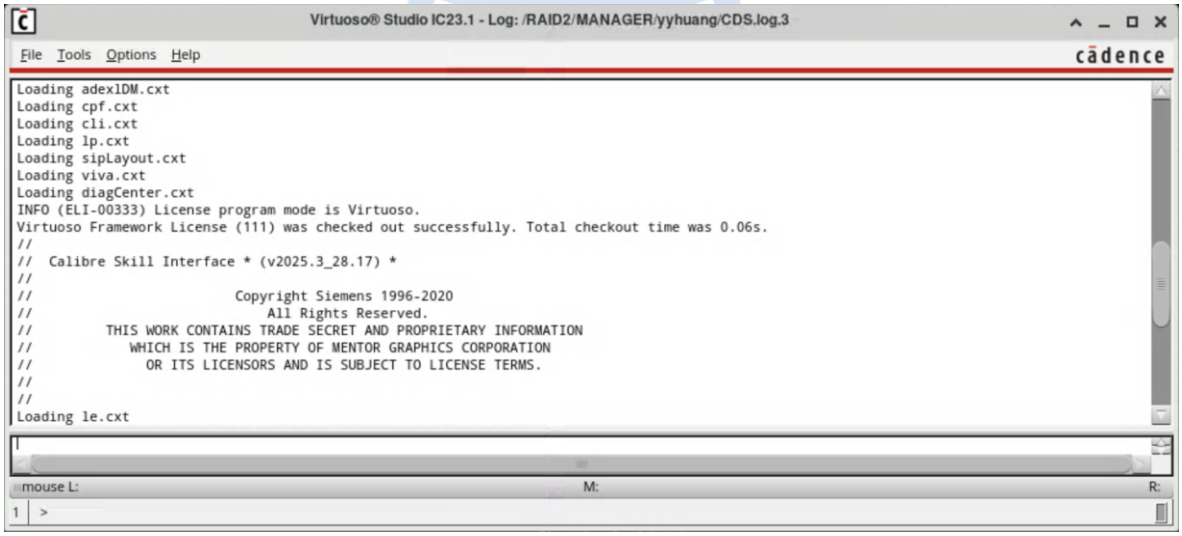
使用以下指令載入 virtuoso 所需環境 * Do This Step Before Using Any Tool

[~/ADFP/N16ADFP_iPDK]$ module load base/fc

[~/ADFP/N16ADFP_iPDK]$ module load virtuoso/23

2.2 打開 Virtuoso 軟體

[~/ADFP/N16ADFP_iPDK]$ virtuoso &

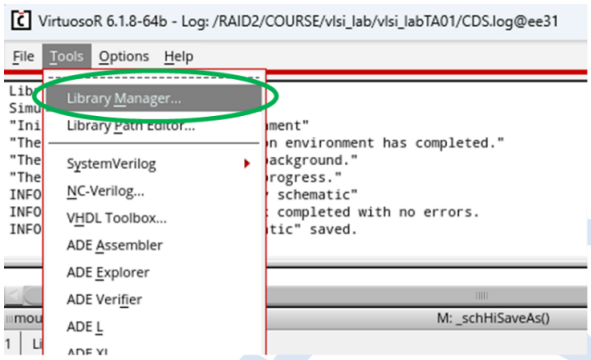


打開的版本應為 IC23.1

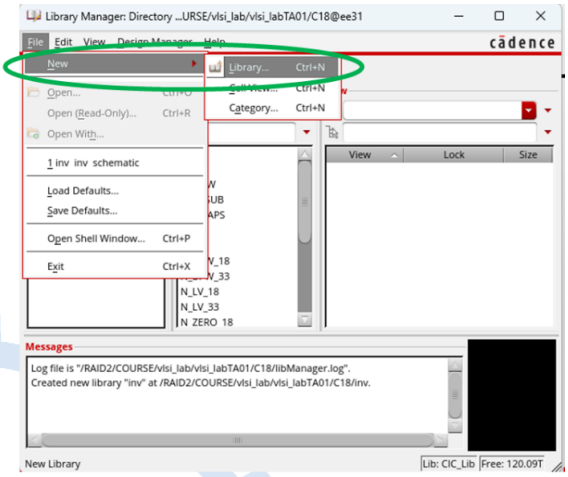
2.3 創建 Library

(1)點選「Tool」→ 「Library Manager」

(2)點選「File」→ 「New」→ 「Library」



(1) Tools -> Library Manager

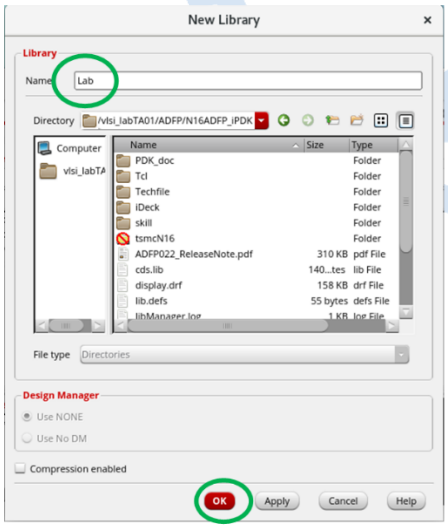


(2) File -> New -> Library

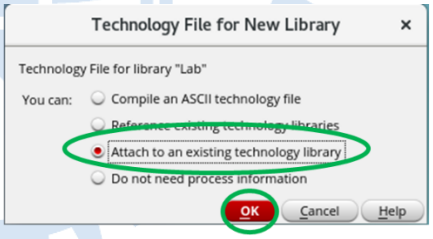
(3)輸入 Library Name (這邊以輸入 “Lab” 示範)

(4)點選「Attach to an existing technology library」→ 「OK」

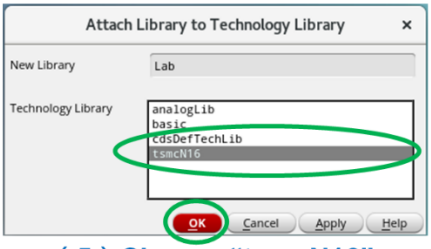
(5)點選「tsmcN16」→ 「OK」



(3) Enter library name “Lab”



(4) Attach to an existing technology library



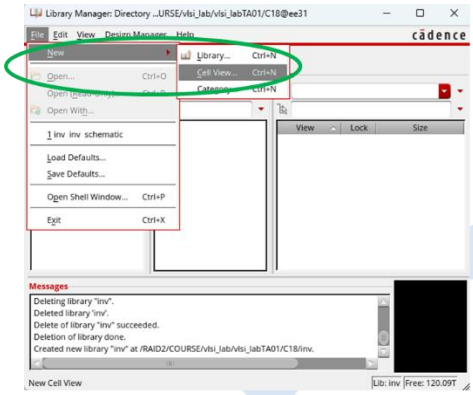
(5) Choose “tsmcN16”

2.4 創建 Schematic

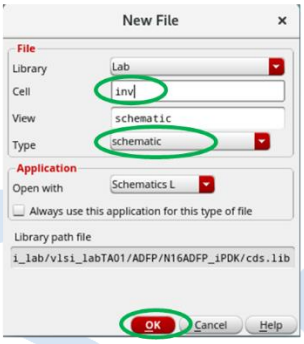
(1)點選「New」→ 「Cell View」

(2)輸入 cell name，點選「schematic」→ 「OK」

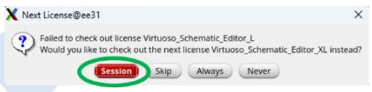
(3)點選「Session」



(1) New -> Cell View



(2) Enter the cell name
Select "schematic"

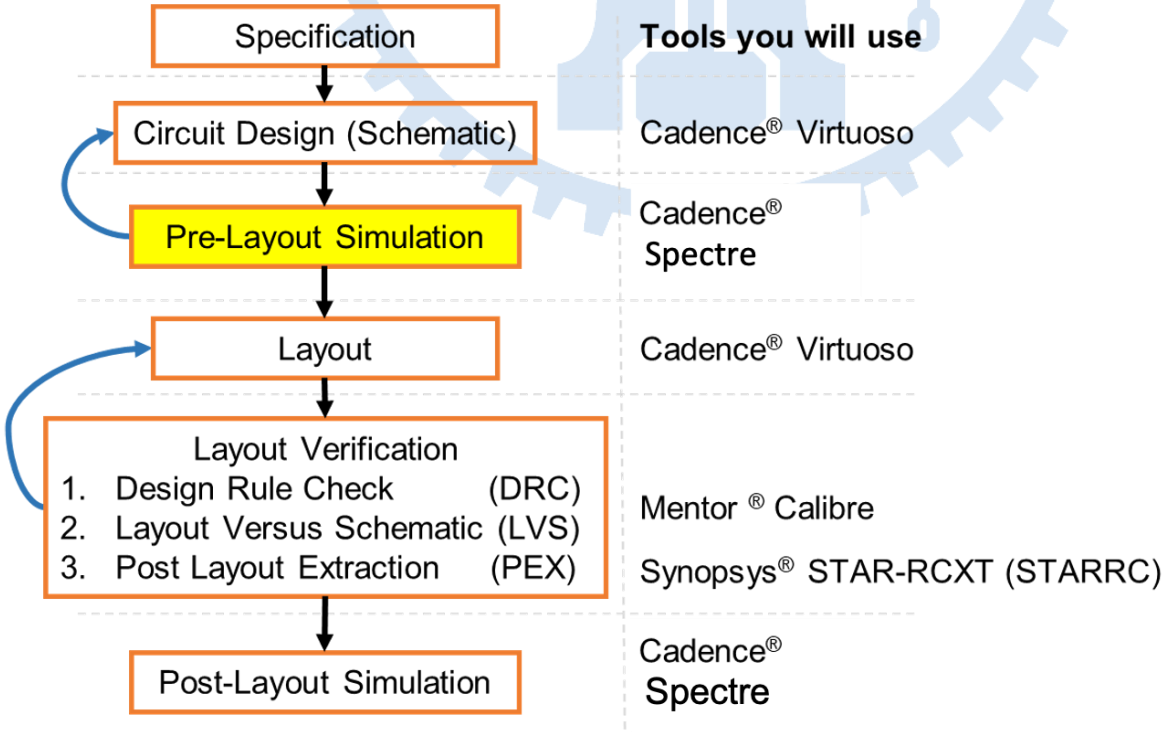


(3) Session

2.5 Create Inverter Schematic / Symbol Design

請根據自行需求繪製 Schematic / Symbol

3. Pre-Layout Simulation (Using spectre)



3.1 建立 testbench

(1)跟剛才創建 schematic 一樣的方式，建立一個你的電路的 testbench

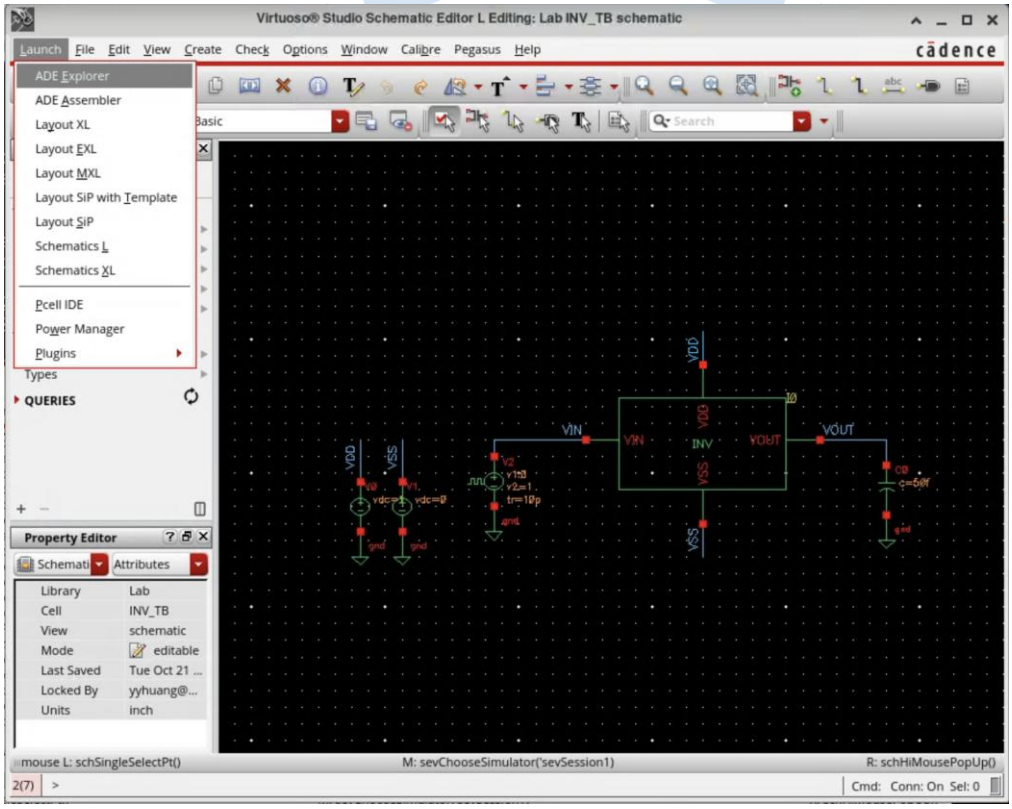
(2)「New」→ 「Cell View」→輸入 cell name，點選「schematic」→ 「OK」

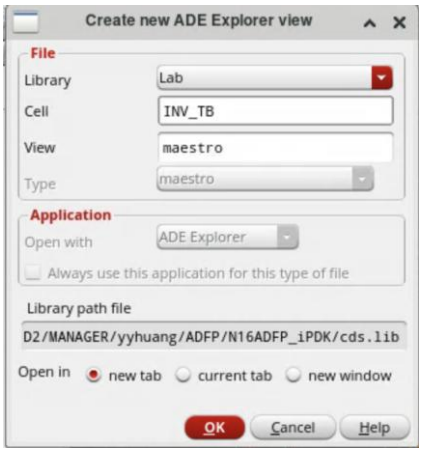
3.2 開啟 ADE 模擬介面

(1)在 testbench schematic 介面點選「Launch」→「ADE Explorer」

(2)若是第一次跑這個 testbench，用 Create New View 創建一個新的

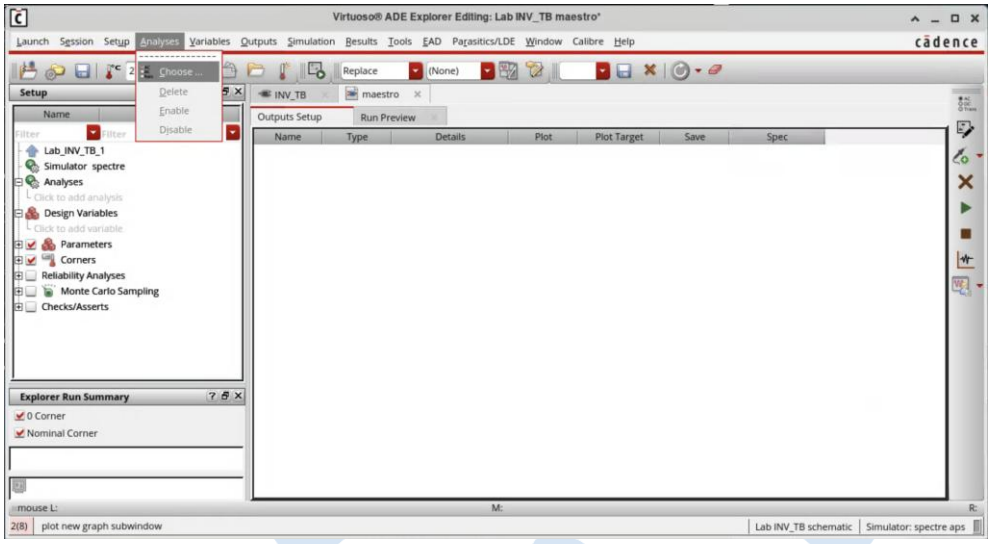
(3)預設 View 的名字為 maestro，點 ok



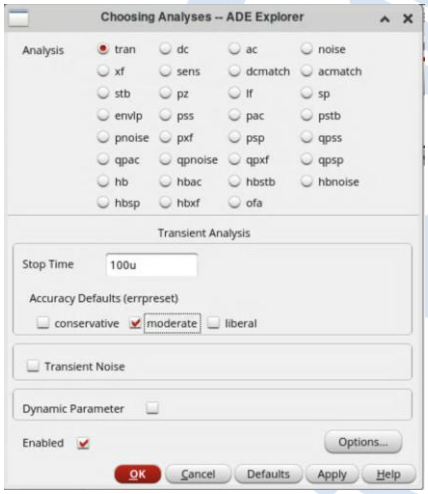


3.3 設定模擬參數

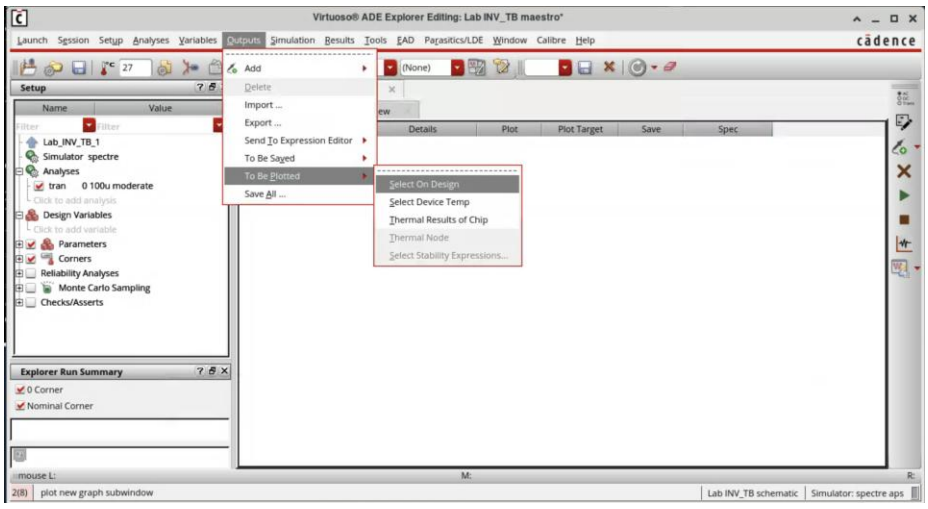
(1)在 ADE Explorer → 「Analyses」→「Choose」選擇要跑的模擬



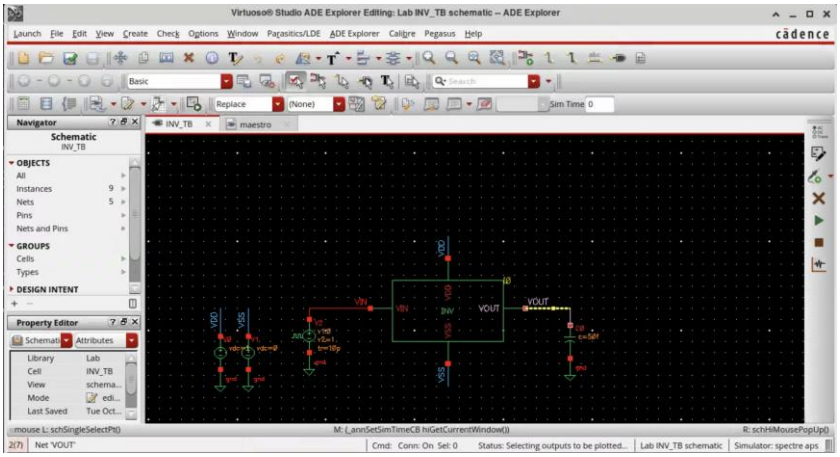
(2)此處以 100us transient 模擬為例



(3)在 ADE Explorer →「Output」→「To Be Plotted」→「Select on Design」

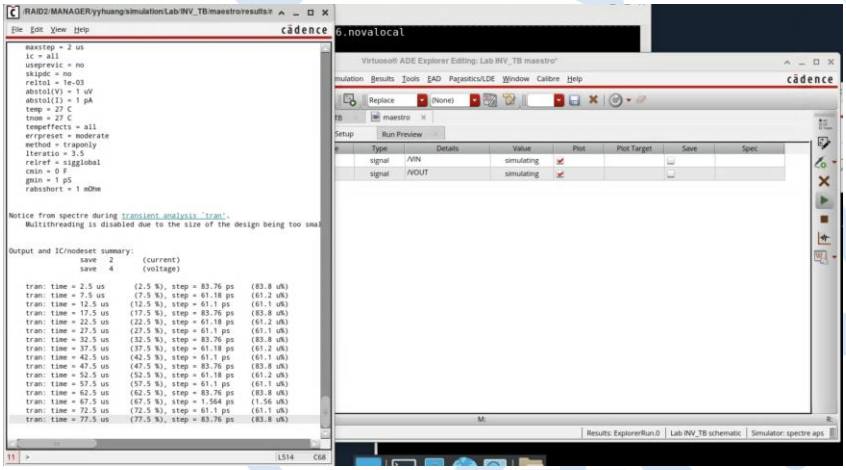


(4)轉跳到 schematic 點選想要觀察的節點位置



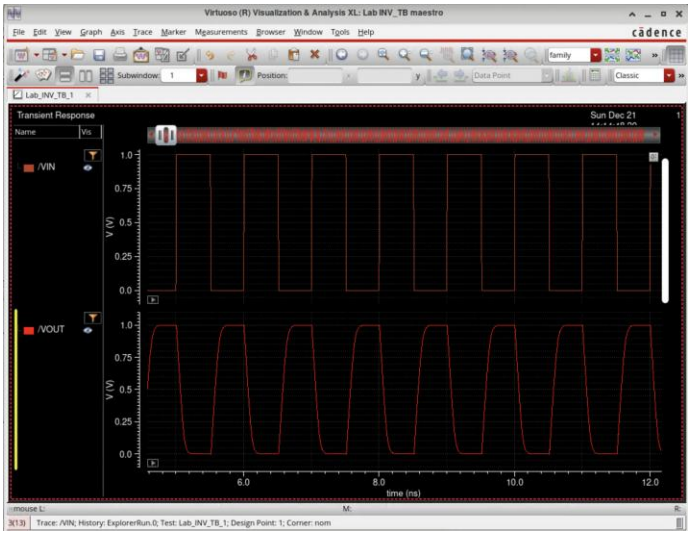
3.4 執行電路模擬

(1)點選 ADE Explorer 視窗右側綠色箭頭開始執行模擬

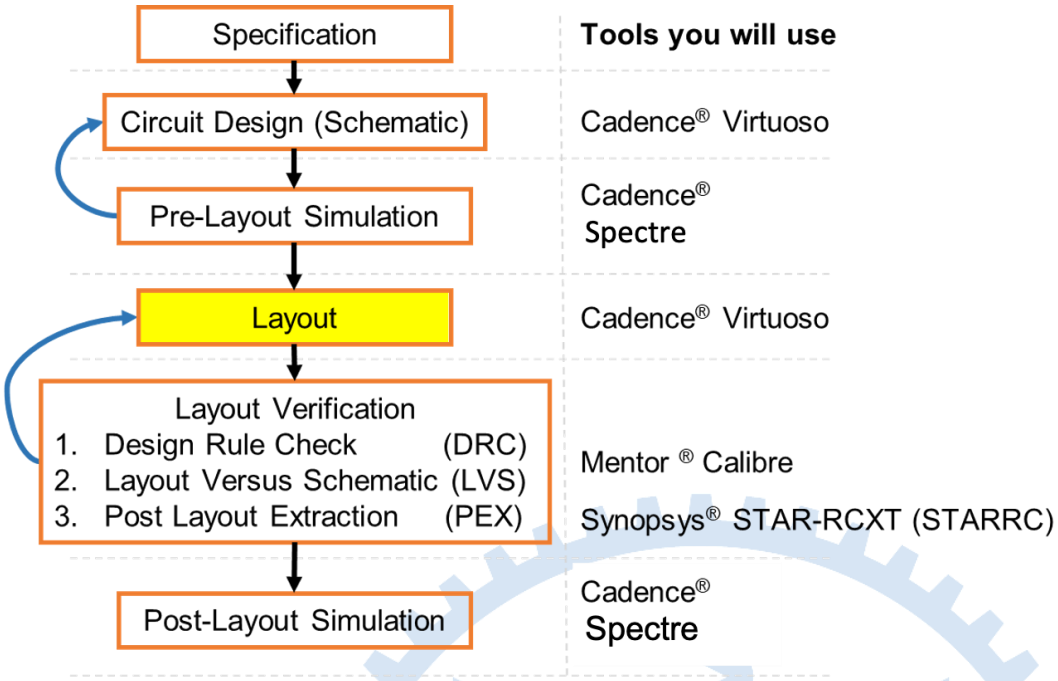


3.5 查看波型

(1)剛剛在模擬之前設定要 plot 的波形會自行顯示出來



4. Layout

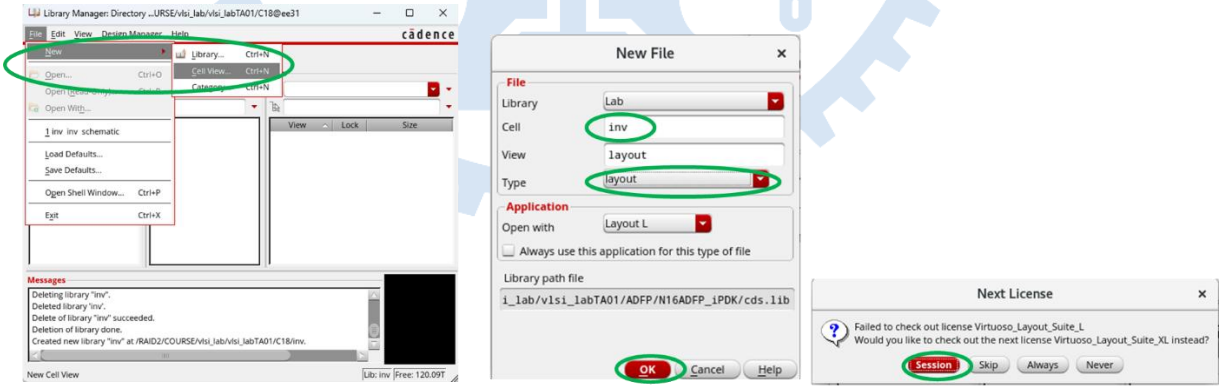


4.1 創建 Layout View

(1)點選「New」→ 「Cell View」

(2)輸入 cell name，點選「layout」→ 「OK」

(3)點選「Session」



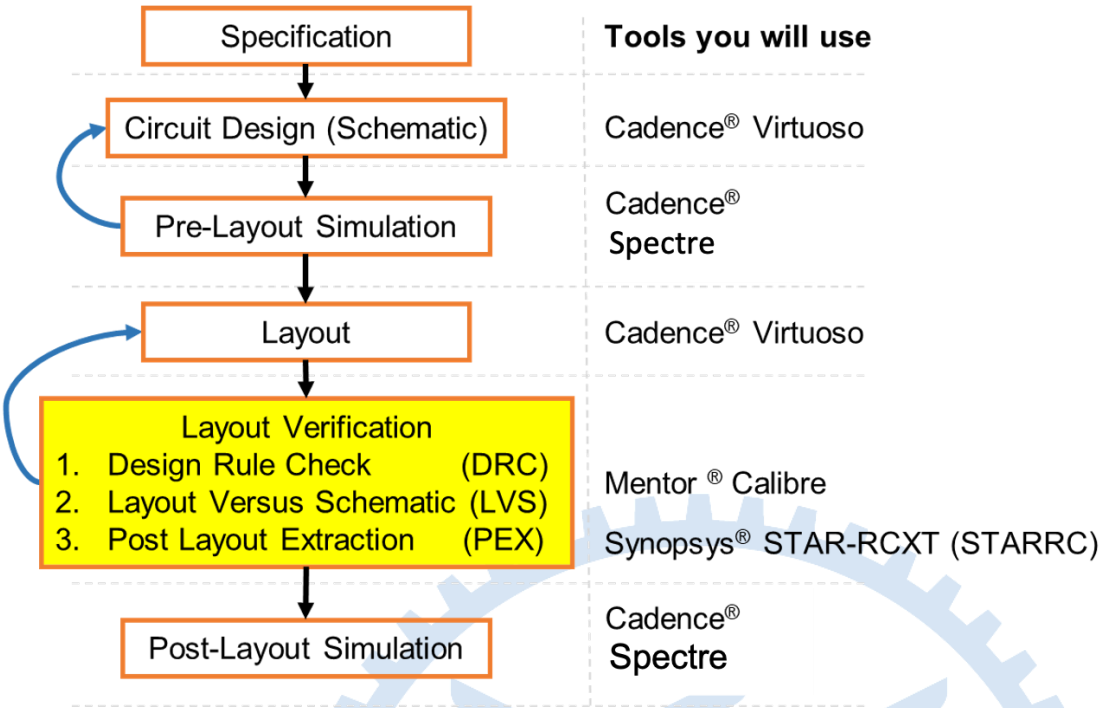
(1) New -> Cell View　(2) Select "Layout"　(3) Session

4.2 Create Inverter Layout Design

請根據自行需求創建，可參考相關課程教學文件

VLSILAB_ADFP_layout_tutorial_2024-01-12.pdf

5. Layout Verification – DRC

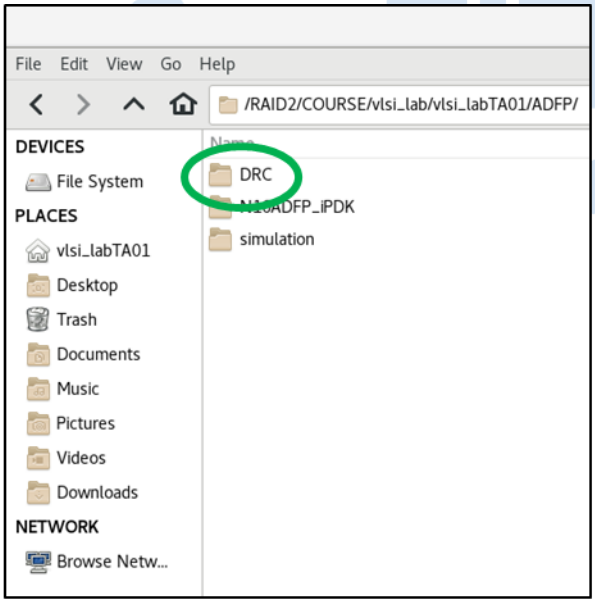


5.1 創建 DRC 資料夾

[~]$ cd ~/ADFP

[~/ADFP]$ mkdir DRC

[~/ADFP]$ cd DRC



(1) Create new folder for DRC

5.2 拷貝 DRC 規則

- **Full-Chip Rule:**

[~/ADFP/DRC]$ cp

/RAID2/PROCESS/ADFP/Executable_Package/Collaterals/Tech/DRC/N16ADFP_DRC_Calibre/LOGIC_TopMr_DRC/N16ADFP_DRC_Calibre_11M.11_1a.encrypt ./

- **Antenna Rule:**

[~/ADFP/DRC]$ cp

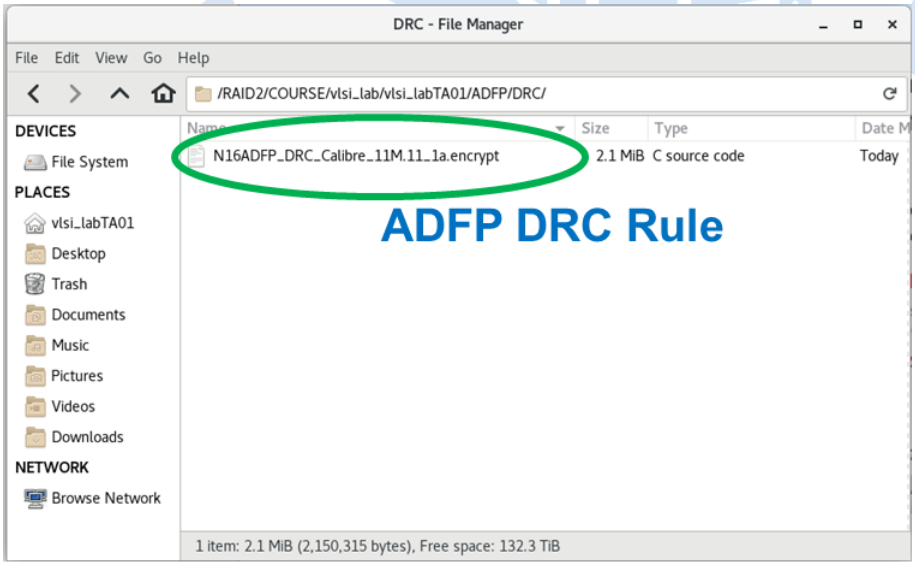
/RAID2/PROCESS/ADFP/Executable_Package/Collaterals/Tech/DRC/N16ADFP_DRC_Calibre/ANTENNA_DRC/N16ADFP_DRC_Calibre_11M_ANT.11_1a.encrypt ./

- **IP-Level Rule:**

[~/ADFP/DRC]$ cp

/RAID2/PROCESS/ADFP/Material/DRC/N16ADFP_DRC_Calibre_11M.11_1a.encrypt ./

一般課程範例建議使用 IP-Level Rule 避免出現一些可在 IP Level 忽略的 DRC，例如: Density Check。



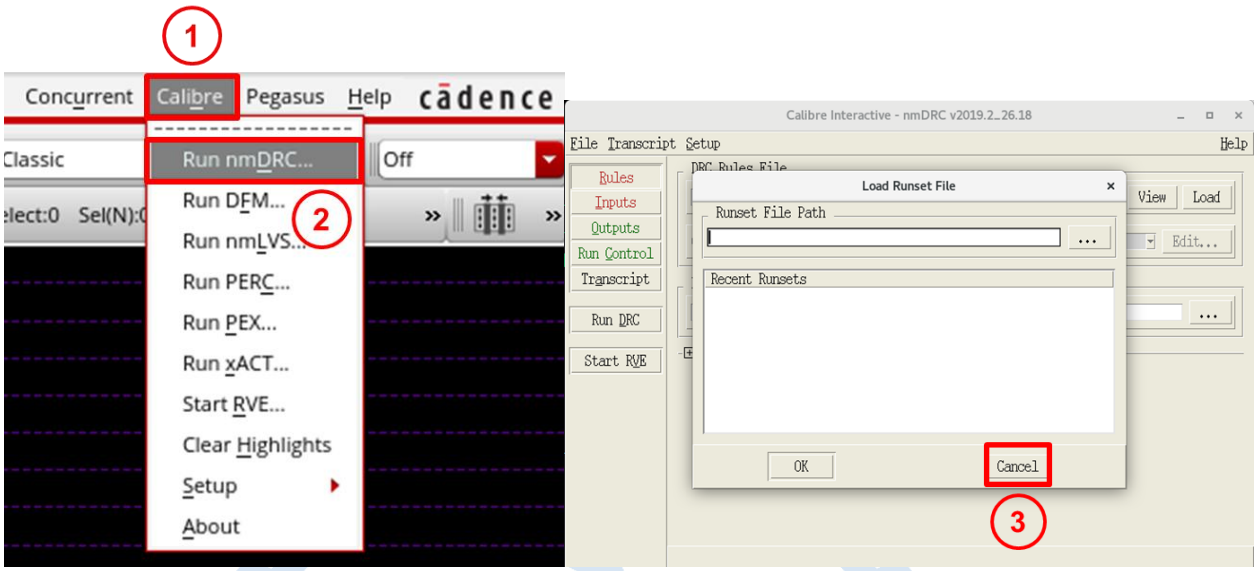
(2) Ensure that DRC rule is copied

如想更了解請參閱家目錄的浮水印文件，有關 DRC Rule 設定:

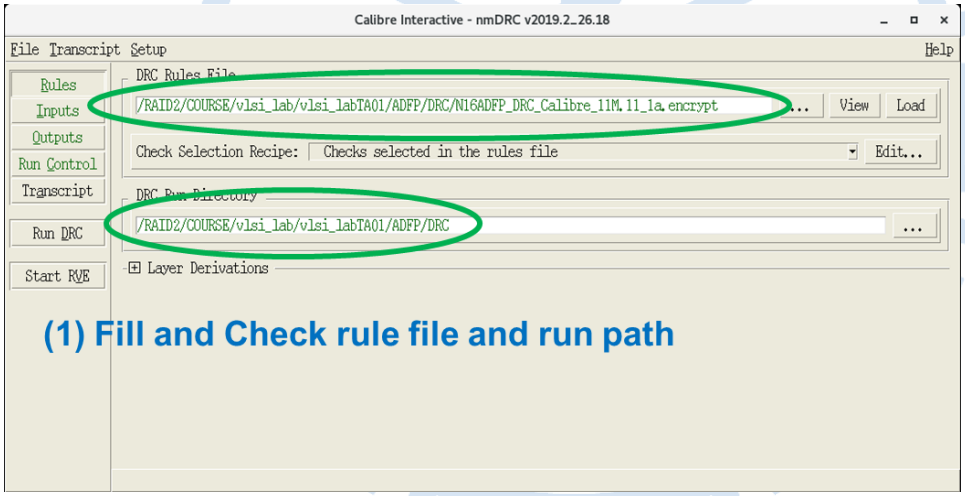
~/Desktop/ADFP_PDF/ADFP040_N16_DRC_Switch_Usage_wmp.pdf

5.3 從 Virtuoso 打開 Calibre

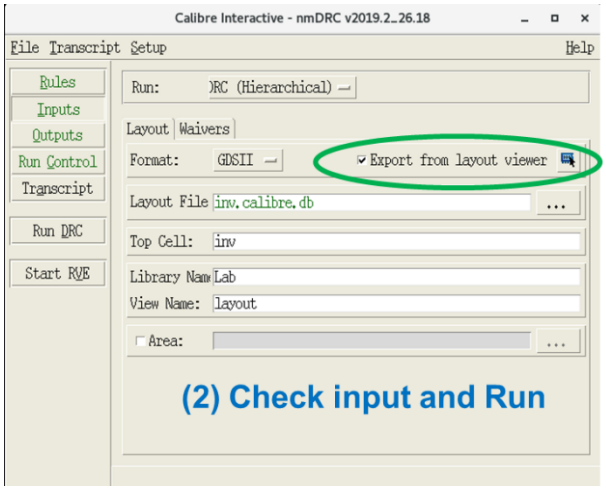
(1)點選「Calibre」→ 「Run nmDRC」→ 「Cancel」



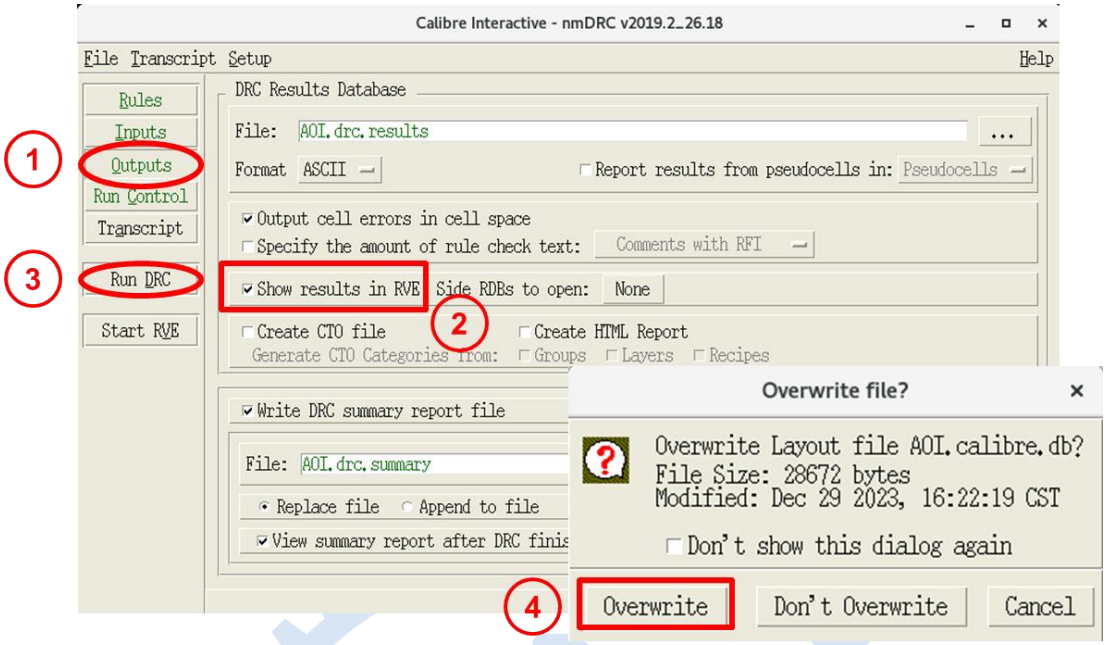
(2)點選「Rules」→ 「Load」→ 「選取剛剛複製過來的 DRC Rule」



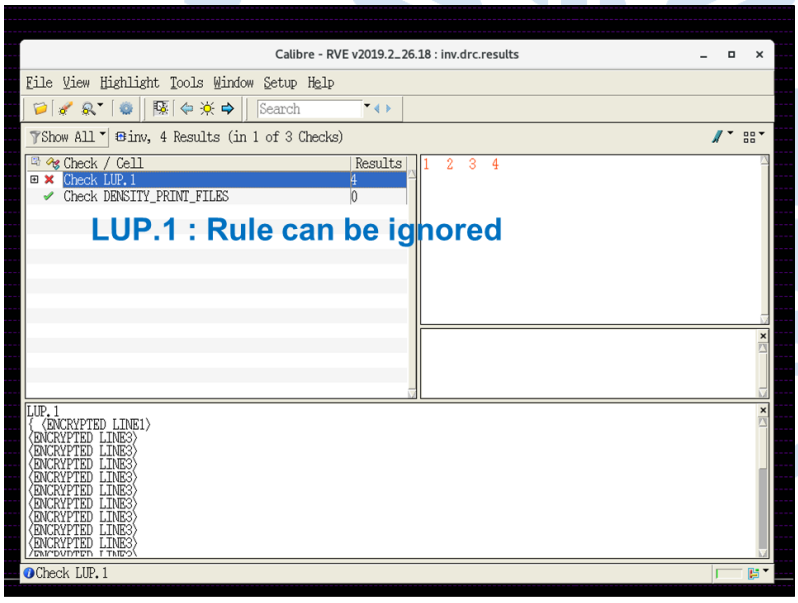
(3)點選「Inputs」→ 勾選「Export from layout viewer」



(4)點選「Outputs」→ 勾選「Show results in RVE」→ 「Run DRC」



5.4 確認 DRC Rule 是哪裡違反



(3) Check DRC Result

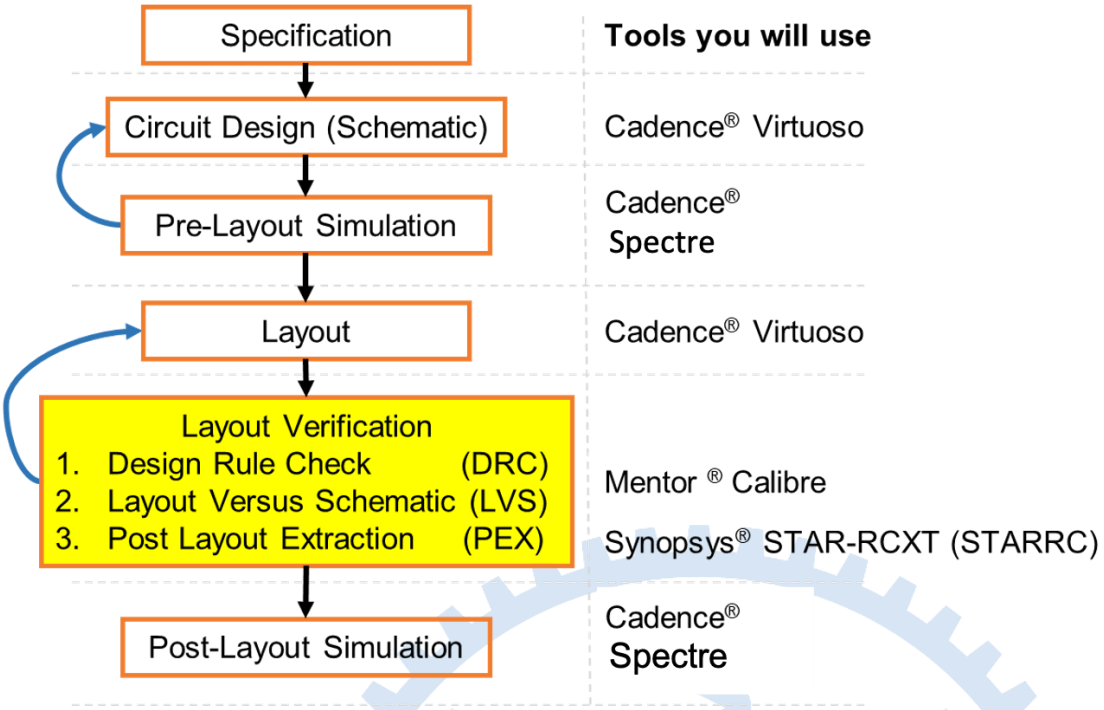
Note: 因 ADFP 的 DRC 有加密，因此違反細節不會顯示在 RVE 當中

如想更了解請參閱家目錄的浮水印文件，有關 DRC Rule 說明:

~/Desktop/ADFP_PDF/ADFP039_N16ADFP_DRM_V1.1_1.pdf

善用 PDF 搜尋功能找到對應的 DRC 規則。

6. Layout Verification – LVS

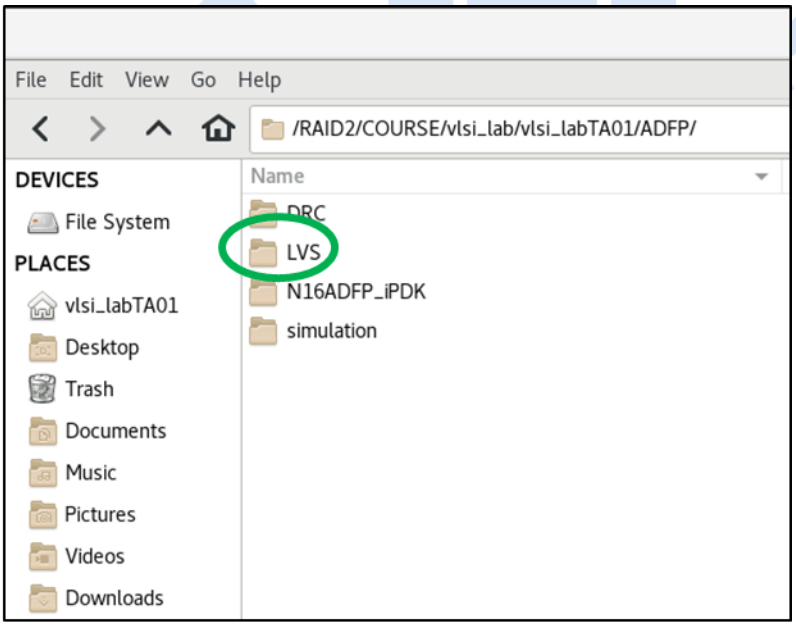


6.1 創建 LVS 資料夾

[~]$ cd ~/ADFP

[~/ADFP]$ mkdir LVS

[~/ADFP]$ cd LVS



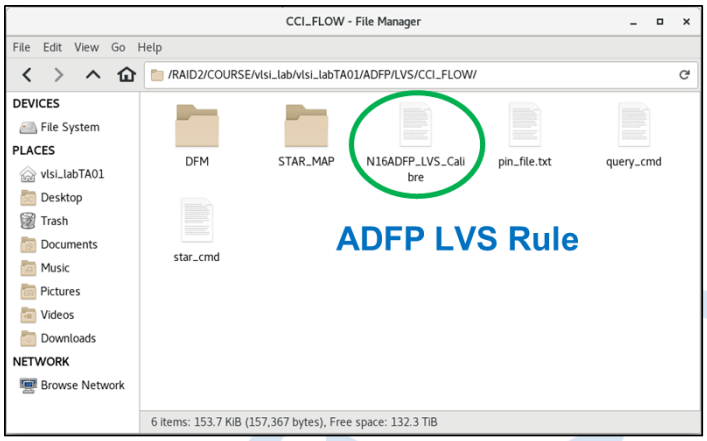
(1) Create new folder for LVS

6.2 拷貝 LVS 規則

LVS Rule:

[~/ADFP/LVS]$ cp -r /RAID2/PROCESS/ADFP/Material/LVS ./

Rule file name: N16ADFP_LVS_Calibre



(2) Ensure whole directory is copied

如想更了解，請使用「MyPDF」參閱浮水印文件，有關 LVS Rule 說明:

ADFP003_N16_ADFP_Calibre_LVS_BOX_Command_Usage.pdf

ADFP004_N16_ADFP_Calibre_LVS_Deck_Usage.pdf

ADFP005_N16_ADFP_Dummy_Pickup_Checking.pdf

ADFP006_N16_ADFP_ERC_Usage.pdf

ADFP007_N16_ADFP_LOD_Measurement.pdf

ADFP008_N16_ADFP_LVS_Filter_Introduction.pdf

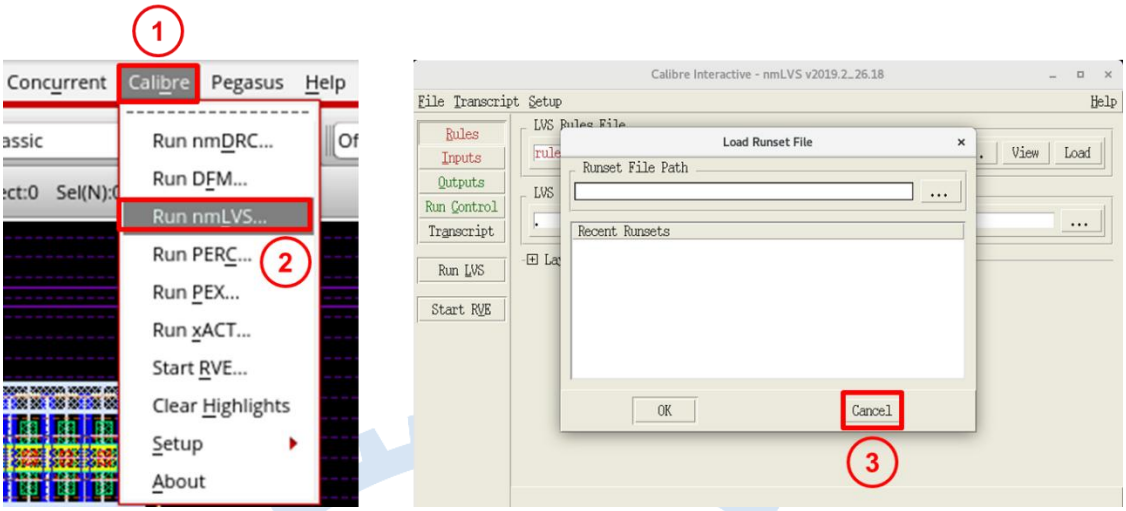
ADFP009_N16_ADFP_NF_MOS_Parallel_Reduction.pdf

ADFP010_N16_ADFP_STD_Filter_Cells.pdf

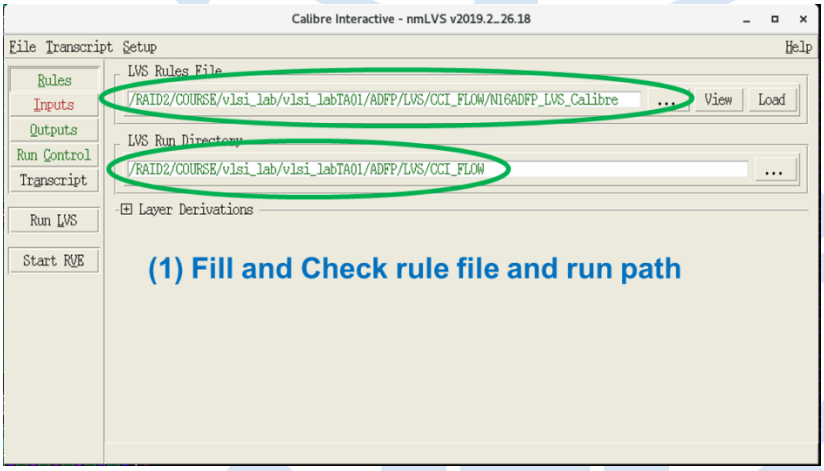
ADFP011_N16_ADFP_Unrecognized_Device.pdf

6.3 從 Virtuoso 打開 Calibre:

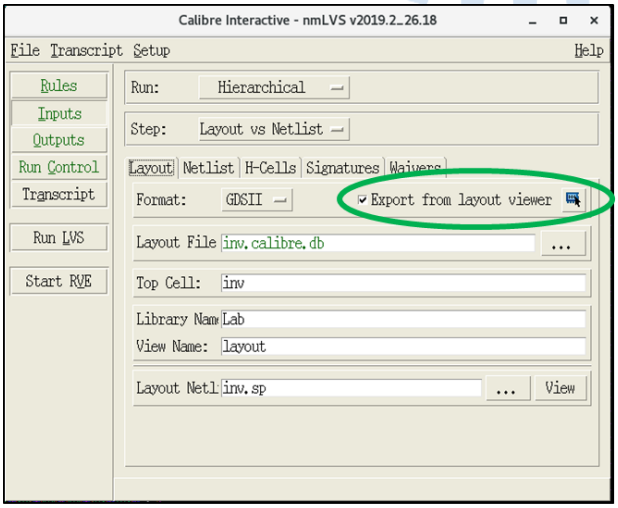
(1)點選「Calibre」→ 「Run nmLVS」→ 「Cancel」



(2)點選「Rules」→「Load」→ 「選取剛剛複製過來的 LVS Rule」



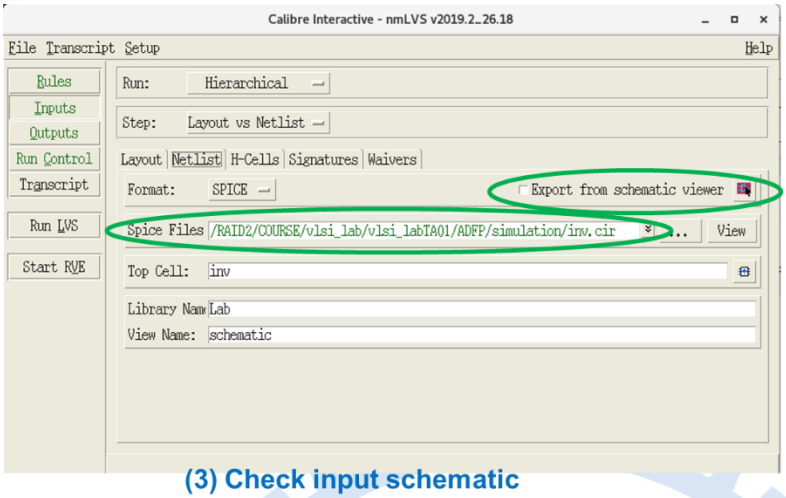
(3)點選「Inputs」→「Layout」→ 勾選「Export from layout viewer」



(2) Check input layout

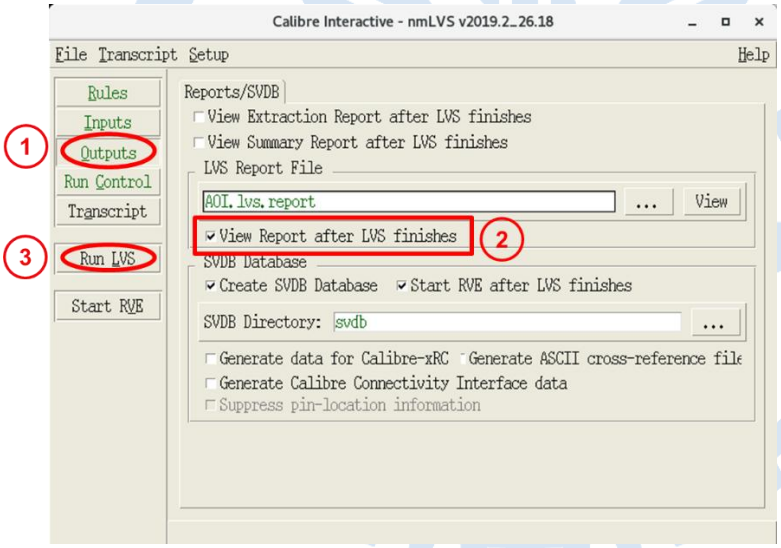
(4)點選「Inputs」→「Netlist」→ 取消勾選「Export from … viewer」

(5)點選「Spice Files 旁的 View」→「選擇 Pre-sim 輸出的 sp 檔案」

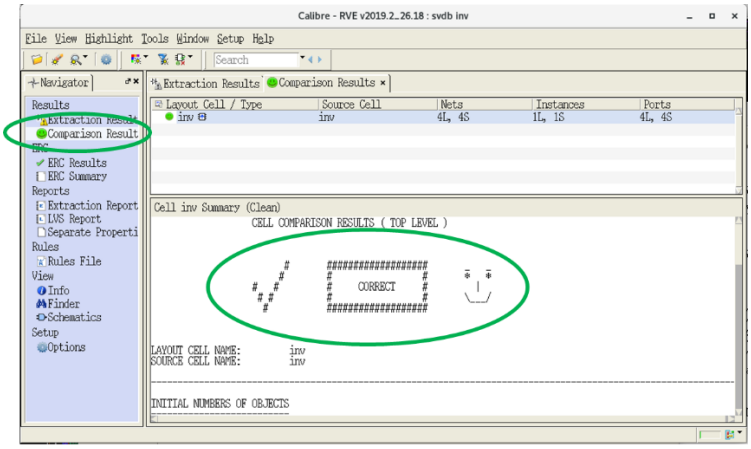


(3) Check input schematic
(Your Pre-Sim Circuit Netlist)

(6)點選「Outputs」→ 勾選「View Report after LVS finishes」→ 「Run LVS」

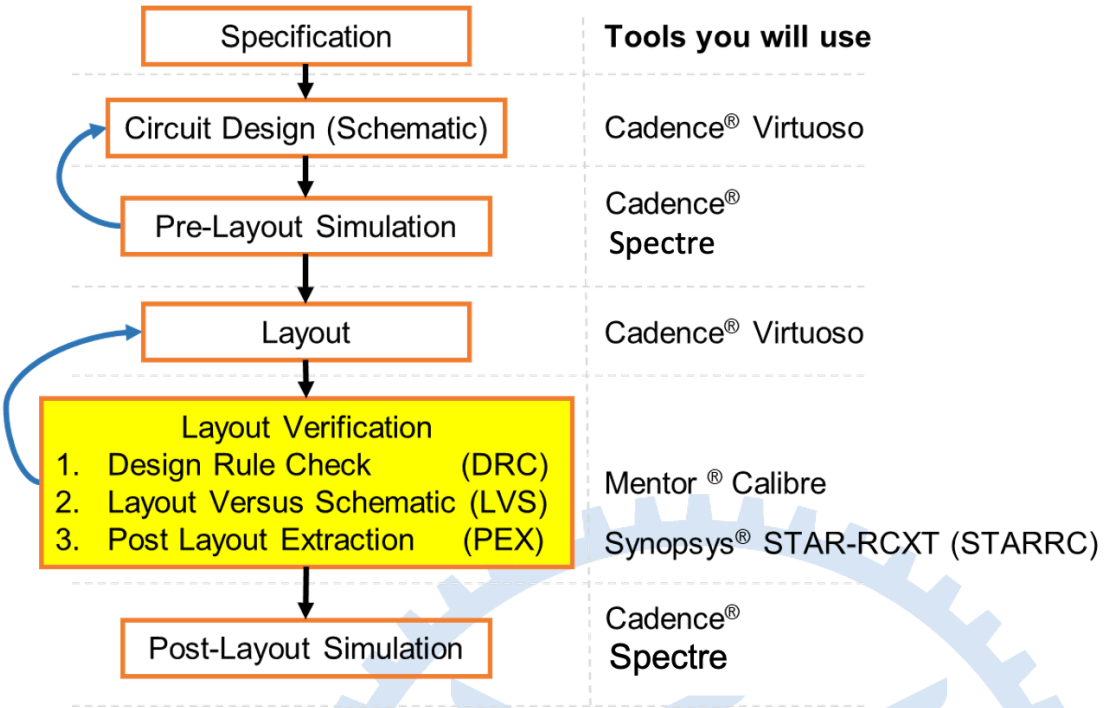


(7)查看 LVS 結果



(5) Check LVS Result

7. Layout Verification – PEX

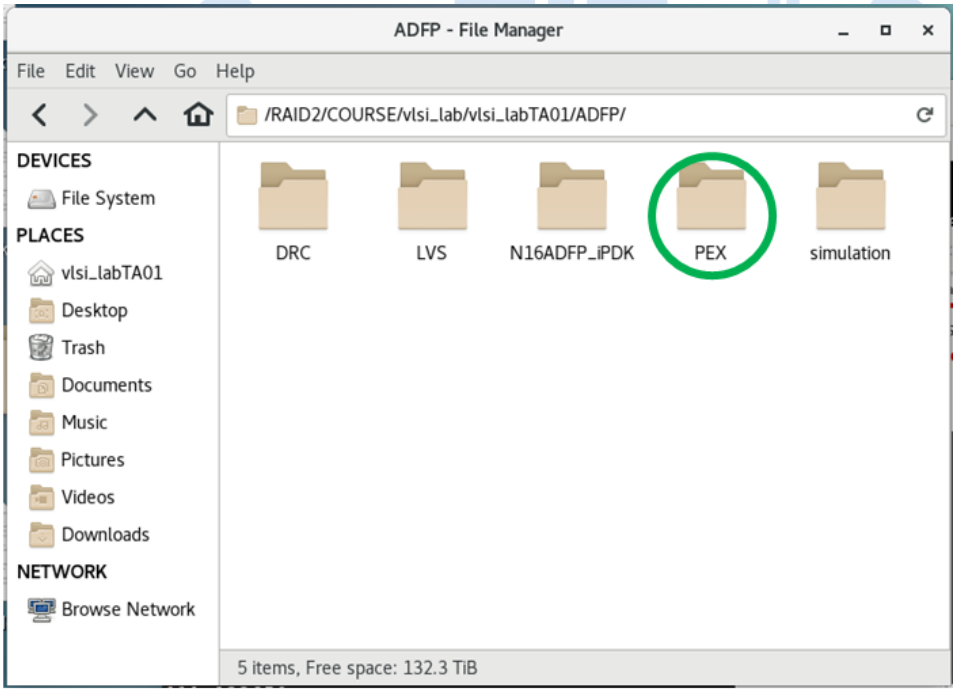


7.1 創建 PEX 資料夾

[~]$ cd ~/ADFP

[~/ADFP]$ mkdir PEX

[~/ADFP]$ cd PEX

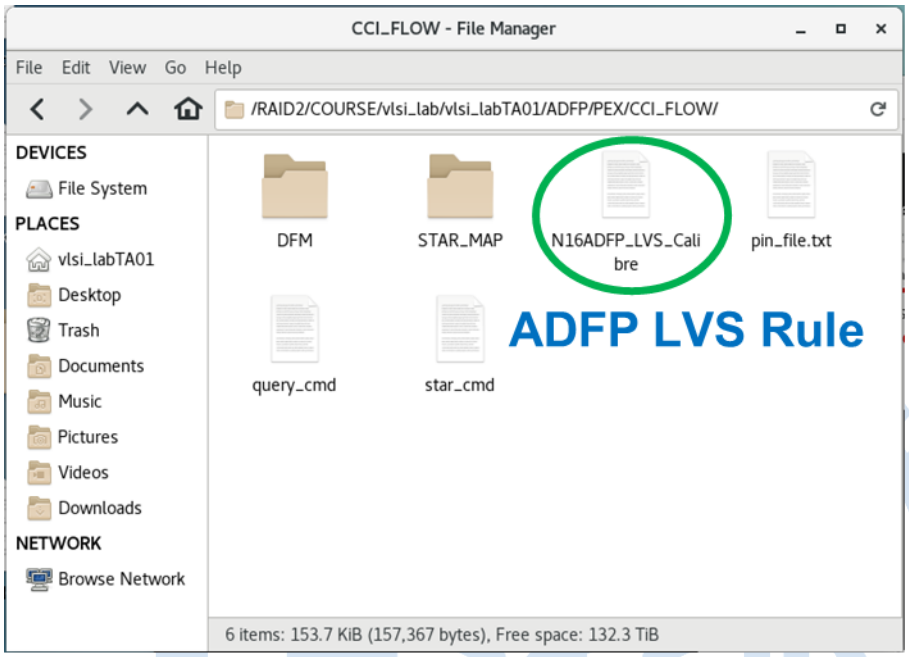


(1) Create new folder for PEX

7.2 拷貝 CCI_Flow 資料夾

[~/ADFP/PEX]$ cp -r /RAID2/PROCESS/ADFP/Material/CCI_FLOW ./

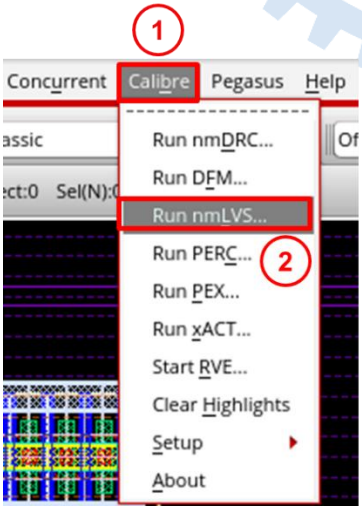
LVS Rule file name: N16ADFP_LVS_Calibre

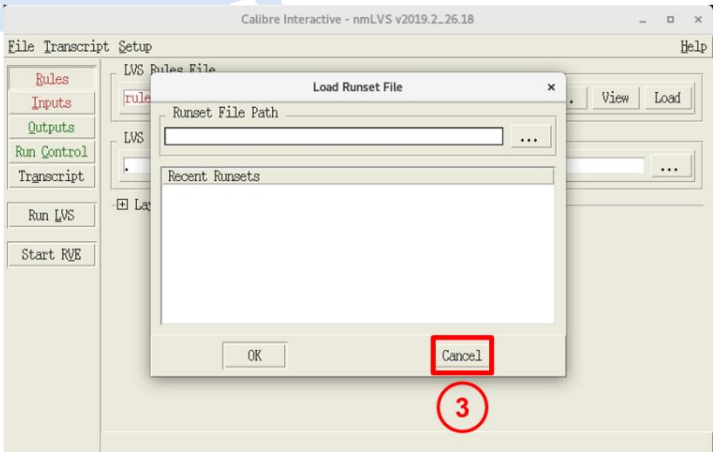


(2) Ensure whole directory is copied

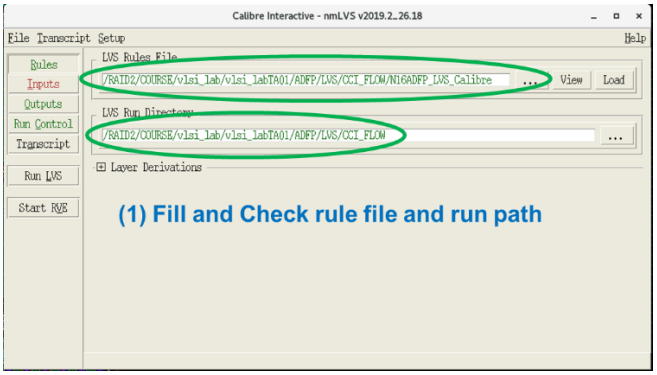
7.3 從 Virtuoso 打開 Calibre LVS，產出 svdb 檔案:

(1)點選「Calibre」→ 「Run nmLVS」→ 「Cancel」

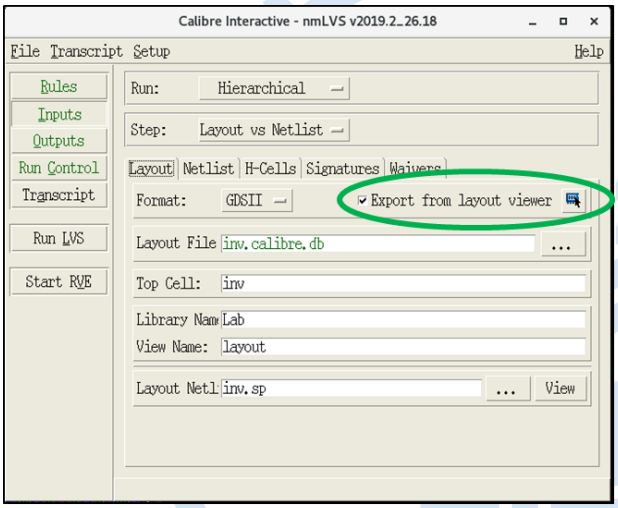




(2)點選「Rules」→「Load」→ 「選取剛剛複製過來的 LVS Rule」



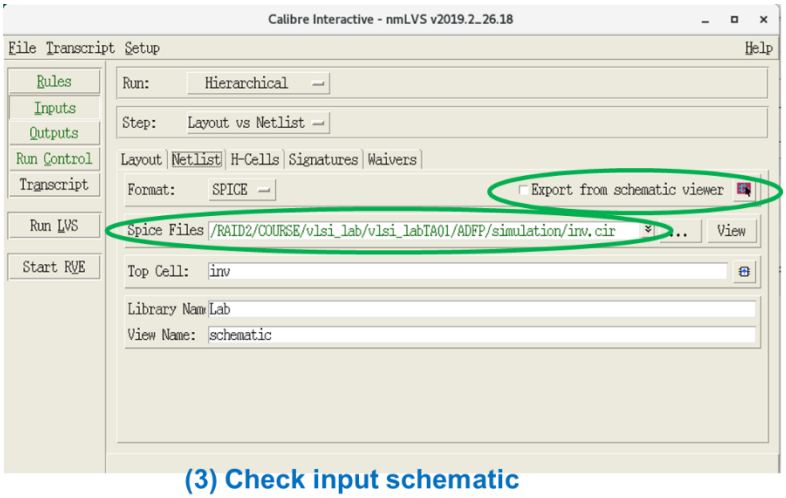
(3)點選「Inputs」→「Layout」→ 勾選「Export from layout viewer」



(2) Check input layout

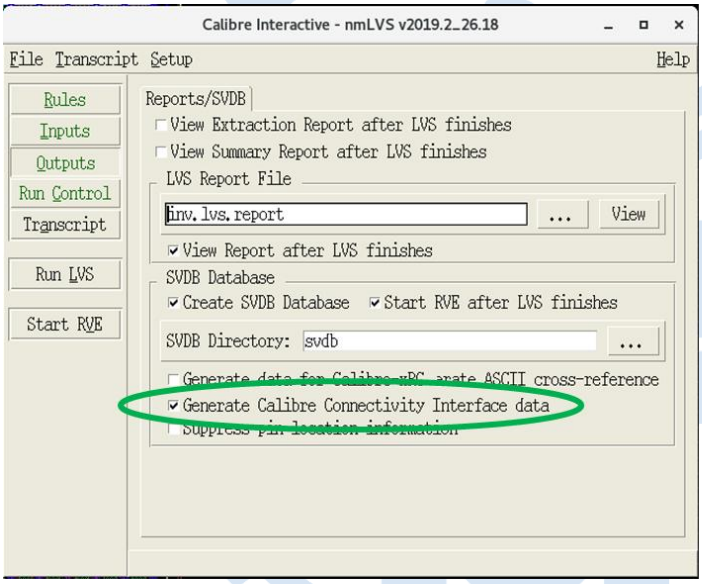
(4)點選「Inputs」→「Netlist」→ 取消勾選「Export from … viewer」

(5)點選「Spice Files 旁的 View」→「選擇 Pre-sim 輸出的 sp 檔案」



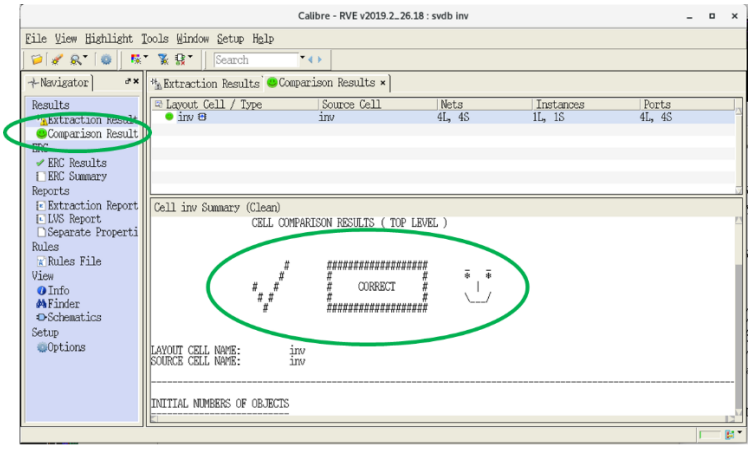
(3) Check input schematic
(Your Pre-Sim Circuit Netlist)

(6)點選「Outputs」→ 勾選「View Report after LVS finishes」→ 勾選「Generate Calibre Connectivity Interface Data」→「Run LVS」



(4) Generate CCI data for STARRC

(7)查看 LVS 結果



(5) Check LVS Result

7.4 使用 query_cmd 將 LVS 輸出檔轉為 StarRC 所需輸入檔

(1)確認 LVS 沒有問題之後，開啟新的 terminal 視窗，載入所需的環境

[~/ADFP/PEX/CCI_FLOW]$ module load base/fc

[~/ADFP/PEX/CCI_FLOW]$ module load virtuoso/23

[~/ADFP/PEX/CCI_FLOW]$ module load starrc/2025

[~/ADFP/PEX/CCI_FLOW]$ calibre -query ./svdb/ < query_cmd

並確認 terminal 中沒有出現 error

7.5 準備其他必要檔案

[~/ADFP/PEX/CCI_FLOW]$ module load starrc/2025

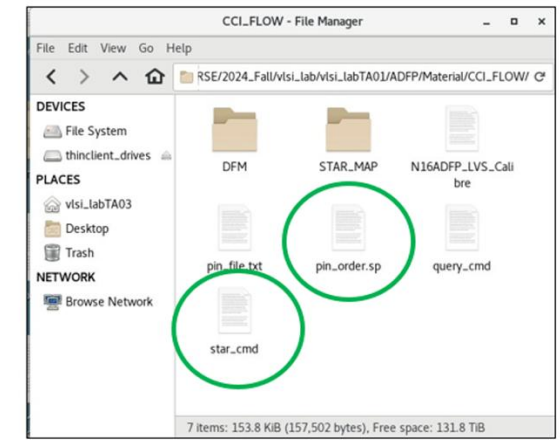
[~/ADFP/PEX/CCI_FLOW]$ cp

/RAID2/PROCESS/ADFP/Material/CCI_FLOW/STAR_MAP/starrcxt_mapping_1p11m ./

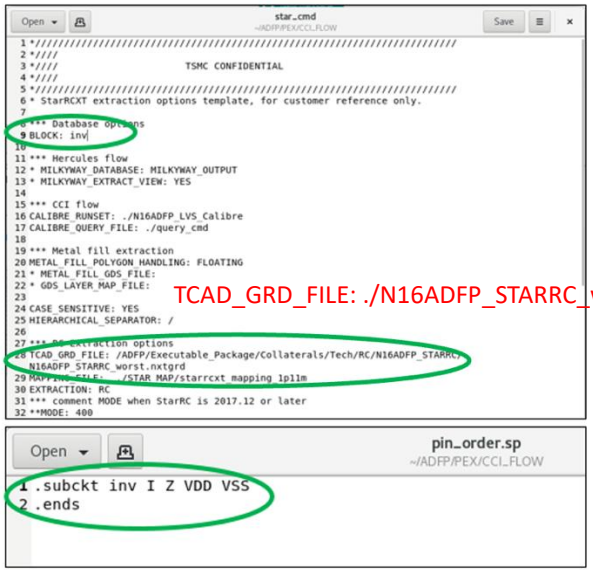
[~/ADFP/PEX/CCI_FLOW]$ cp /RAID2/PROCESS/ADFP/

Executable_Package/Collaterals/Tech/RC/N16ADFP_STARRC/N16ADFP_STARRC_worst.nxtgrd ./

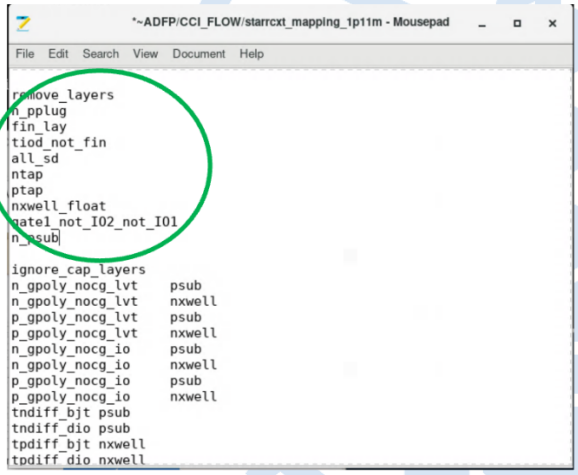
7.6 針對欲抽取電路更改 star_cmd, starrcxt_mapping_1p11m 與 pin_order.sp 內容



Modify "star_cmd" and "pin_order.sp"



Change Top Cell Name and Sub-Circuit Definition

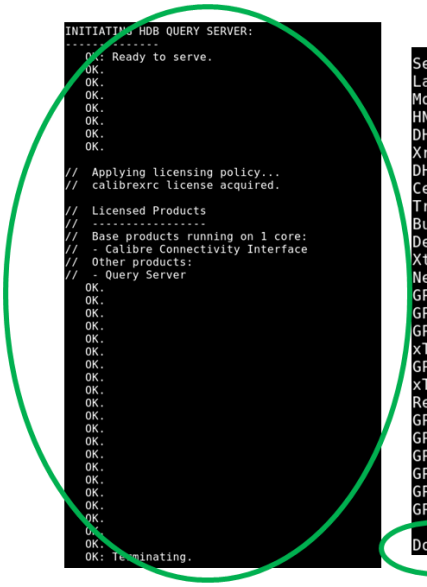


In starrxt_mapping file, add the following to the "remove layers" list:
ntap, ptap, nxwell_float, gate1_not_IO2_not_IO1, n_psub

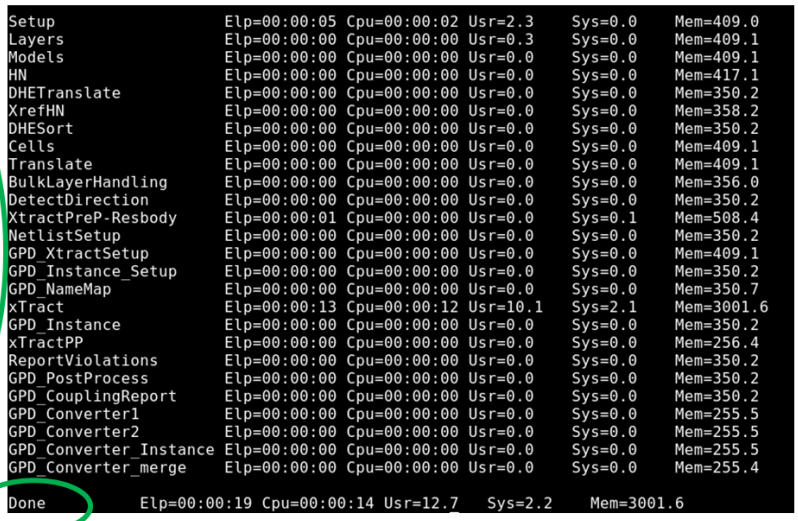
7.7 根據 star_cmd 內容抽取寄生電路

(若使用新開啟的 terminal 記得一樣要 module load)

[~/ADFP/PEX/CCI_FLOW]$ StarXtract -clean star_cmd

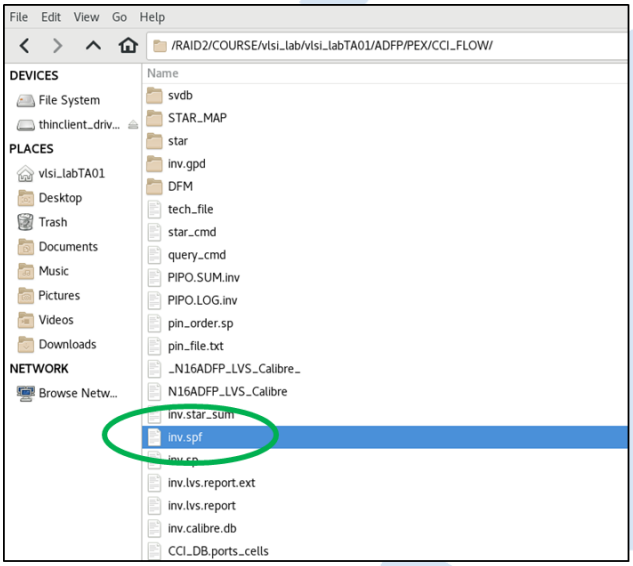


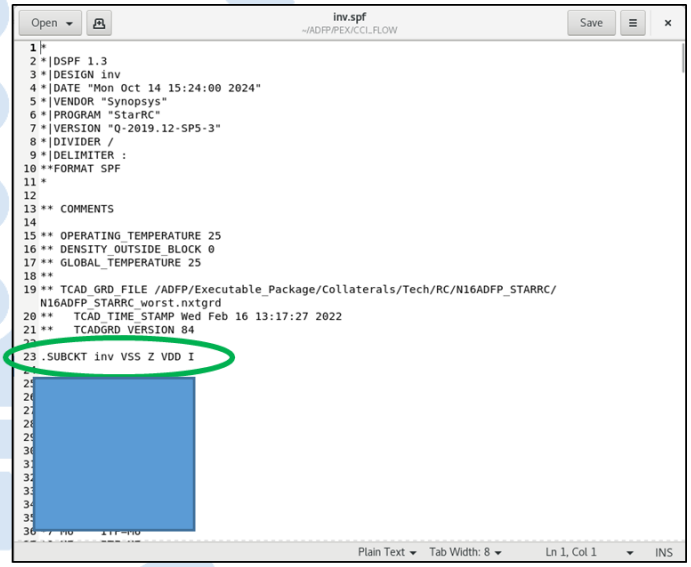
Query Result



Star-RC Result

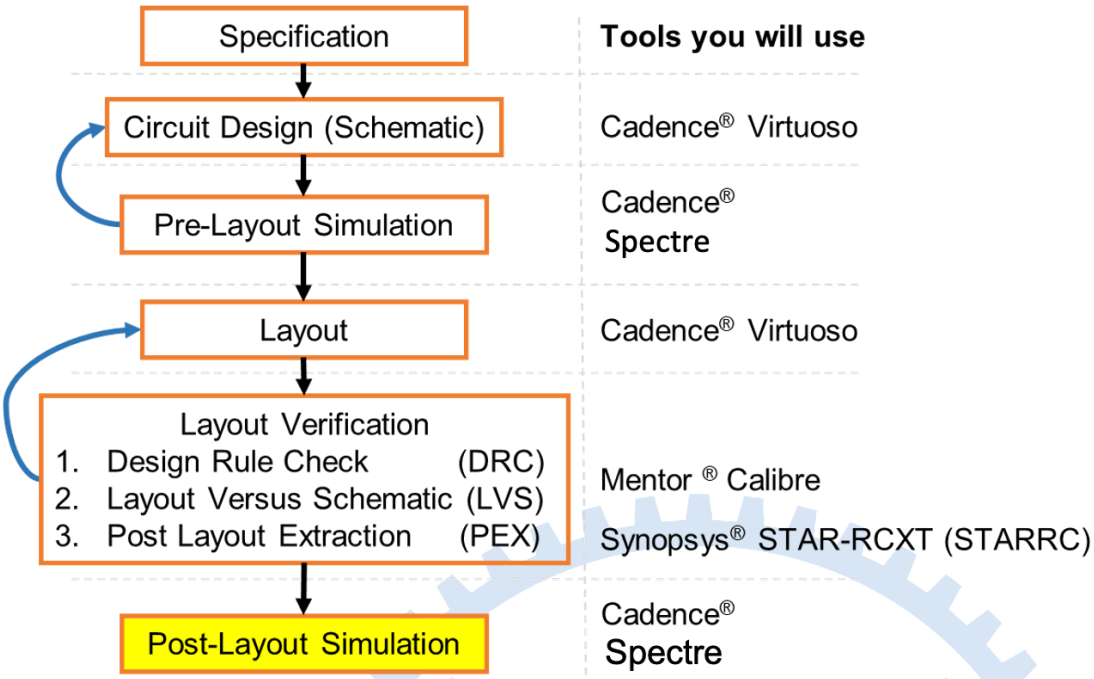
7.8 查看 Extract 出的寄生電路





Extracted Netlist

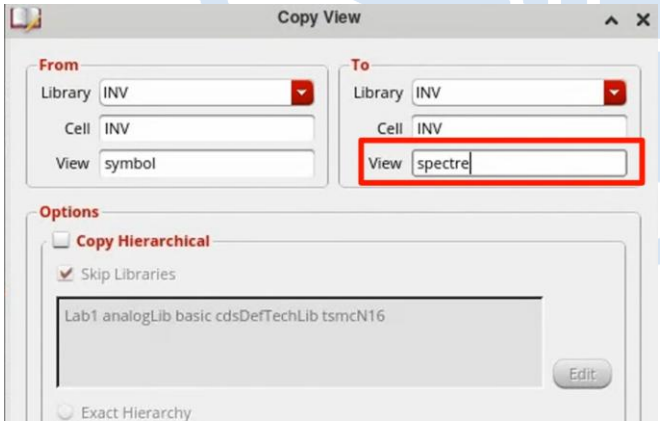
8. Post-Layout Simulation



8.1 創建 post-sim 所需的 Spectre cellview

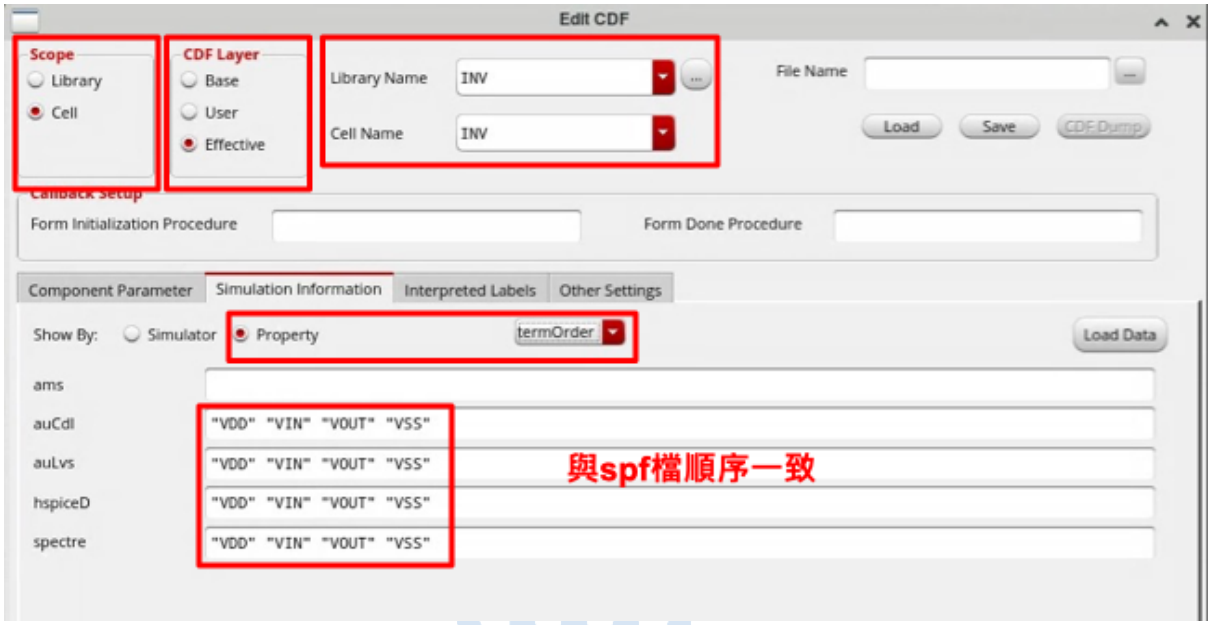
(1)在 Virtuoso Library Manager 中對 Cell 的 symbol 按右鍵複製

(2) View 改成 spectre



(3) 此時 cell 內應該要有 layout、schematic、spectre、 symbol 等檔案

(4) 從 Virtuoso 點選「Tools」 → 「CDF」→「Edit」，根據先前產生的.spf 檔案設定 Pin 腳順序

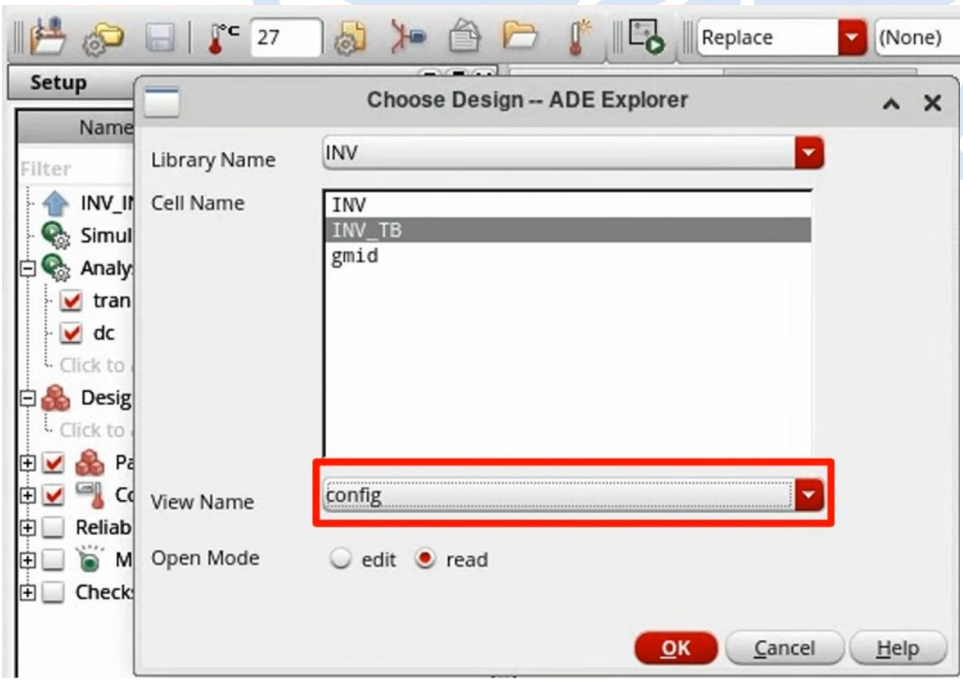


8.2 修改 TestBench 以使用新的 post-sim spectre 檔案

(1) 在 testbench cell 中創建新的 cell view, type 選 config

(2) 在剛剛跑完 PEX 的 cell 上面點選右鍵→「Set Cell View」→ 「Specify SPCE Source File」，Source file 選擇/PEX/CCI_FLOW 中的 spf 檔並存檔

8.3 使用 ADE 跑模擬，Post-sim 的時候 ADE Assembler 記得改成 config



8.4 與先前的 pre-sim 相同，若有事先設定好想要 plot 的訊號節點，模擬結束後波形會自動顯示

9. 查看 TSMC 提供之 FC 文件範例練習

9.1 請使用「MyPDF 

」參閱相關浮水印文件，有關 FC 說明：

(1) ADFP046_TSMC_N16ADFP_Introduction_20220118_wmc.pdf

有關 TSMC ADFP 製程的簡要說明。

(2) ADFP044_TSMC_N16ADFP_Layout_20220118_wmc.pdf

有關 2D-Planner 和 FinFET Layout 的理論介紹和差異(圖解)

以及特別的 DRC Rule 和 Layer 層說明。

(3) ADFP042_TSMC_N16ADFP_Lab_Layout_20220211_wmc.pdf

該文件提供 Lab 練習，使用 Layout Tool 繪製基本邏輯閘。

(4) ADFP047_TSMC_N16ADFP_SPICE_20220118_wmc.pdf

有關 Spice model 的說明。

10. 查看 NYCU 課程提供之 FC 文件範例練習

10.1 請使用「MyPDF 

」參閱相關浮水印文件，有關 FC 說明：

(1) VLSILAB_ADFP_full_custom_tutorial_2024-01-12.pdf

有關 TSMC ADFP 製程的簡要說明。有關 2D-Planner 和 FinFET Layout 的理論介紹和差異(圖解)以及特別的 DRC Rule 和 Layer 層說明。

(2) VLSILAB_ADFP_layout_tutorial_2024-01-12.pdf

有關如何「善用」ADFP 各層來實現 AOI 數位邏輯閘。

Revision Record and Author List

Original Tutorial by 施品辰、莊勝傑、蕭邦原

2024.11.18 Version 1 edited by Lin-Hung Lai

2025.12.19 Version 1 edited by Yen-Yun Huang

2026.03.08 Version 2 edited by Bang-Yuan Xiao